AMENDEMNTS TO THE CLAIMS

Please amend independent claims 1, 6 and 14 in accordance with the following:

1. (Currently Amended) A receiving circuit for measuring a bit error rate characteristic, comprising:

a demodulator circuit demodulating a radio signal in a digital communication system that includes a burst signal and outputting the demodulated data therefrom;

a detector which detects a synchronizing pattern included in the demodulated data and outputs an instruction signal for providing instructions for a result of the detection;

a pulse generator capable of receiving the instruction signal and outputting a pulse signal each time a predetermined time elapses since the reception of the instruction signal;

a control circuit which outputs control signals corresponding to at least either one of the instruction signal and the pulse signal; and

a clock generator which generates a clock signal for storing and outputting a pseudo random pattern ~~desired data~~ included in the demodulated data in response to the control signal.

2. (Original) The receiving circuit as claimed in claim 1, further including a pulse transfer control circuit which receives the pulse signal therein and controls the transfer of a signal corresponding to the pulse signal to said control circuit according to a mode signal.

3. (Original) The receiving circuit as claimed in claim 1, wherein said pulse generator comprises a counter which performs counting based on an operating clock signal used to operate said receiving circuit, and further including a clock transfer control circuit which receives the operating clock signal therein and controls the transfer of a signal corresponding to the operating clock signal to said pulse generator according to a mode signal.

4. (Previously Presented) The receiving circuit as claimed in claim 2, wherein said mode signal specifies a normal operating mode at a first voltage level and specifies a bit error rate measuring mode at a second voltage level different from the first voltage level,

and said pulse transfer control circuit restrains the transfer of a signal corresponding to the pulse signal to said control circuit when the mode signal is of the first voltage level and permits the transfer of the signal corresponding to the pulse signal to said control circuit when the mode signal is of the second voltage level.

5. (Previously Presented) The receiving circuit as claimed in claim 3, wherein said mode signal specifies a normal operating mode at a first voltage level and specifies a bit error rate measuring mode at a second voltage level different from the first voltage level, and said clock transfer control circuit restrains the transfer of a transferring signal corresponding to the operating clock signal to said pulse generator when the mode signal is of the first voltage level and permits the transfer of the transferring signal corresponding to the operating clock signal to said pulse generator when the mode signal is of the second voltage level.

6. (Currently Amended) A radio signal receiving circuit <u>for measuring a bit error rate characteristic,</u> comprising:

a demodulator circuit demodulating a burst signal in a digital communication system that is included in a radio signal received by the demodulator circuit, the demodulator circuit outputting demodulated data;

a detector detecting a synchronizing pattern signal from the demodulated data received thereto;

a pulse generator generating a pulse signal in response to the synchronizing pattern signal;

a control circuit generating a control signal in response to the synchronizing pattern signal and the pulse signal;

a clock generator outputting a clock signal in response to the control signal; and

a storing circuit storing and outputting <u>a pseudo random pattern included in</u> the demodulated data in response to the clock signal.

7. (Previously Presented) A radio signal receiving circuit according to claim 6, wherein the burst signal includes a preamble, a unique word, an error detection bit and data.

8. (Previously Presented) A radio signal receiving circuit according to claim 7, wherein the unique word corresponds to the synchronizing pattern signal.

9. (Previously Presented) A radio signal receiving circuit according to claim 6, wherein the pulse generator includes a counter.

10. (Previously Presented) A radio signal receiving circuit according to claim 6, wherein the pulse generator generates the pulse signal when either one of the synchronizing pattern signal or the pulse signal is activated.

11. (Previously Presented) A radio signal receiving circuit according to claim 6, wherein the clock signal includes a first clock signal and a second clock signal.

12. (Previously Presented) A radio signal receiving circuit according to claim 6, wherein the pulse generator outputs the pulse signal at a timing after a predetermined time has passed from receiving the synchronizing pattern signal.

13. (Previously Presented) A radio signal receiving circuit according to claim 12, wherein the predetermined time is about 5 microseconds.

14. (Previously Presented) A radio signal receiving circuit for measuring a bit error rate characteristic, comprising:

a demodulator circuit receiving a radio signal that includes a burst signal, the demodulator circuit generating demodulated data by demodulating the burst signal;

a detector connected to the demodulator circuit, the detector outputting a synchronizing pattern signal detected from the demodulated data;

a pulse generator connected to the detector, the pulse generator generating a pulse signal in response to the synchronizing pattern signal;

a control circuit connected to the detector and the pulse generator, the control circuit outputting a control signal in response to the synchronizing pattern signal and the pulse signal;

a clock generator connected to the control circuit, the clock generator generating a clock signal in response to the control signal; and

a storing circuit connected to the demodulator and the clock generator, the storing circuit storing and outputting a pseudo random pattern included in the demodulated data in response to the clock signal.

15. (Previously Presented) A radio signal receiving circuit according to claim 14, wherein the burst signal includes a preamble, a unique word, an error detection bit and data.

16. (Previously Presented) A radio signal receiving circuit according to claim 15, wherein the unique word corresponds to the synchronizing pattern signal.

17. (Previously Presented) A radio signal receiving circuit according to claim 14, wherein the pulse generator includes a counter.

18. (Previously Presented) A radio signal receiving circuit according to claim 14, wherein the pulse generator generates the pulse signal when either one of the synchronizing pattern signal or the pulse signal is activated.

19. (Previously Presented) A radio signal receiving circuit according to claim 14, wherein the pulse generator outputting the pulse signal at a timing after a predetermined time has passed from receiving the synchronizing pattern signal.

20. (Previously Presented) A radio signal receiving circuit according to claim 19, wherein the predetermined time is about 5 microseconds.